Ins A7

Sub A8

CLAIMS

1. A processor integrated circuit capable of executing more than one instruction stream comprising:

a first processor, coupled to fetch instructions and access data through a first cache controller;

a second processor, coupled to fetch instructions and access data through a second cache controller;

a plurality of cache memory blocks, each containing data memory;

a high-speed interconnect coupling the plurality of cache memory blocks to the first and second cache controllers such that at least one allocable cache memory block is capable of being used by the first and second cache controllers; and

a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, wherein the accessing cache memory controller has access to the allocable cache memory block.

2. The processor integrated circuit of Claim 1, further comprising a plurality of first level cache systems, wherein the first processor fetches instructions and accesses data from the first cache controller through a first first level cache system, and wherein the second processor fetches instructions and accesses data from the second cache controller through a second first level cache system.

3. The processor integrated circuit of Claim 1, wherein the cache memory blocks further comprise cache tag memory.

4. The processor integrated circuit of Claim 1, wherein each cache controller is provided with cache hit rate monitoring apparatus.

5. A method of dynamically allocating cache on a multiple-processor integrated circuit, where the multiple processor integrated circuit is used in a partitionable multiple-processor system and comprises:

a plurality of processors each coupled to receive instructions from a first level cache associated therewith,

a plurality of allocable upper level cache memory blocks,

interconnect apparatus for transmitting cache misses at each first level cache to upper level cache memory blocks assigned thereto, and

allocation apparatus for assigning upper level cache memory blocks to processors;

the method comprising the steps of:

monitoring past cache performance associated with processors and partitions;

determining desired processor to partition and upper level cache block allocations to processors;

repartitioning the system, the step of repartitioning the system including allocation of upper level cache blocks to processors of at least one of the multiple processor integrated circuits.

Sub A8

6. The method of claim 5, wherein the upper level cache blocks are second level cache blocks.

7. The method of Claim 5, further comprising the step of billing customers according to processor time and allocated cache.

8. The method of Claim 5, wherein the multiple processor integrated circuit further comprises a plurality of non-allocable cache memory blocks.

9. The method of Claim 5, wherein the interconnect apparatus further comprises a plurality of upper level cache controllers, and where each upper level cache controller is capable of controlling operation of the allocable cache memory blocks as a writeback cache.

10. The method of Claim 5, wherein each upper level allocable cache block further comprises tag memory and cache data memory.

11. The method of Claim 10, further comprising the steps of stopping 308 execution of operating systems in each partition, and restarting 314 execution of operating systems in each partition, and wherein the system is capable of being repartitioned without rebooting each operating system.